IN THE CLAIMS

What is claimed is:

1. A mask identification circuit, comprising:

a plurality of links arranged in series, each link having at least two inputs and at least two outputs, the inputs being directly coupled to the outputs in a first configuration, the inputs being cross coupled to the outputs in a second configuration.

2. The mask identification circuit of claim 1, wherein:

each link includes at least two conductive lines, the two conductive lines of a link having a first orientation in the first configuration and a second orientation in the second configuration.

3. The mask identification circuit of claim 2, wherein:

the two conductive lines of at least one link are parallel to one another in the first and second configuration.

4. The mask identification circuit of claim 1, wherein:

each link is formed on a different integrated circuit layer.

5. The mask identification circuit of claim 1, wherein:

at least one link includes a first conductive line and a second conductive line, each conductive line having a downward contact to a link formed on a lower integrated circuit layer and an upward contact to a link formed on a higher integrated circuit layer.

6. The mask identification circuit of claim 5, wherein:

the upward contacts are diagonal to one another.

7. The mask identification circuit of claim 1, wherein:

the lower contacts are diagonal to one another.

8. A mask identification code circuit, comprising:

n mask identification (ID) bit circuits that each provide one bit of a mask identification code, where n is an integer greater than 1, and the mask ID bit circuits can provide more than n different mask identification codes.

9. The mask identification code circuit of claim 8, wherein:

each mask ID bit circuit includes a sense node that is coupled to one of at least two different potentials by at least two signal paths.

10. The mask identification code circuit of claim 8, wherein:

each mask ID bit circuit includes a sense node that is coupled to a first potential to identify one mask, to a second potential to identify a second mask and to the first potential to identify a third mask.

11. The mask identification code circuit of claim 8, wherein:

each mask ID bit circuit includes a plurality of separate signal paths cross coupled with one another to identify different masks.

12. The mask identification code circuit of claim 8, wherein:

each mask identification circuit includes a plurality of links, each link being formed on a different integrated circuit layer.

13. The mask identification code circuit of claim 12, wherein:

each link of a mask identification circuit switches the potential supplied to the sense node when switched between configurations, each link including two conductive lines that are each coupled to a conductive line of another link by only one contact in both a first and second configuration.

14. The mask identification code circuit of claim 8, wherein:

the mask ID bit circuits can provide 2^n different mask identification codes with any combination of mask layer revisions.

15. A method for identifying integrated circuit masks, comprising the steps of:

forming mask bit identification (ID) circuits having interconnected links on a plurality of integrated circuit layers that provide a signal path to a sense node, each link being switchable between at least two configurations; and

switching more than one link of a mask bit ID circuit from one configuration to another to represent multiple mask changes.

16. The method of claim 15, wherein:

forming interconnected links includes forming two conductive lines for each link, each conductive line having an upward contact and a downward contact, the upward contacts of the two conductive lines being essentially diagonal to one another, the downward contacts of the two conductive lines being essentially diagonal to one another.

17. The method of claim 15, wherein:

switching a link from one configuration to another includes changing the orientation of two conductive lines of the link.

18. The method of claim 17, wherein:

changing the orientation of the two conductive lines includes placing the two conductive lines essentially perpendicular to a previous orientation.

19. The method of claim 15, wherein:

switching more than one link of a mask ID bit circuit includes switching the configuration of one link for one mask change and switching the configuration of a different link of the same mask ID bit circuit for another mask change.

20. The method of claim 15, wherein:

the links include one link comprising a polysilicon layer and another link comprising an interconnect layer formed over the polysilicon layer.

21. A mask revision identification (ID) code circuit, comprising:

means for cross coupling at least two signal lines according to changes in at least two integrated circuit masks to generate a mask ID code bit.